

REVISIONS

| LTR | DESCRIPTION | DATE (YR-MO-DA) | APPROVED |
|-----|--|-----------------|------------|
| A | Add device types 03-06. Add U package. Changes to Table I and Figures 1, 3, and 4. Editorial changes throughout. | 93-02-19 | M. A. Frye |

| | | | | | | | | | | | | | | | | | | | | |
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| REV | | | | | | | | | | | | | | | | | | | | |
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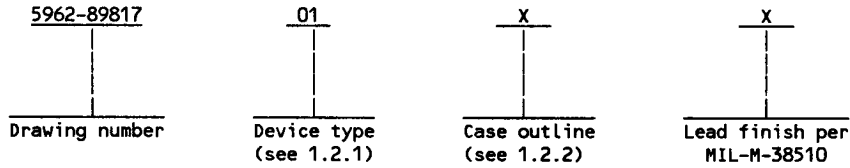
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|----------------------|-------|---|---|---|---|---|---|---|---|---|----|----|----|---|---|--|--|
| REV STATUS OF SHEETS | REV | A | A | A | A | A | A | A | A | A | A | A | A | A | A | | |
| | SHEET | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | | | | |

| | | | | | | | |
|--|-----------------------------------|---|---|--|---------------|--------------------|------------|
| <p align="center">STANDARDIZED MILITARY DRAWING</p> <p>THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE</p> <p>AMSC N/A</p> | PMIC N/A | PREPARED BY Gary L. Gross | DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444 | | | | |
| | CHECKED BY Ray Monnin | MICROCIRCUITS, MEMORY, DIGITAL, CMOS 32K X 8-BIT UVEPROM, MONOLITHIC SILICON | | | | | |
| | APPROVED BY Michael A. Frye | | | | SIZE A | CAGE CODE 67268 | 5962-89817 |
| | DRAWING APPROVAL DATE 91-03-29 | | | | SHEET 1 OF 12 | | |
| | REVISION LEVEL A | 9 | | | | | |

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:



1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

| <u>Device type</u> | <u>Generic number 1/</u> | <u>Circuit function</u> | <u>Access time</u> |
|--------------------|--------------------------|-------------------------|--------------------|
| 01 | | 32K x 8 UVEPROM | 55 ns |
| 02 | | 32K x 8 UVEPROM | 45 ns |
| 03 | | 32K x 8 UVEPROM | 35 ns |
| 04 | | 32K x 8 UVEPROM | 55 ns |
| 05 | | 32K x 8 UVEPROM | 45 ns |
| 06 | | 32K x 8 UVEPROM | 35 ns |

1.2.2 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

| <u>Outline letter</u> | <u>Descriptive designator</u> | <u>Terminals</u> | <u>Package style</u> |
|-----------------------|-------------------------------|------------------|---|
| X | GDIP4-T28 or CDIP3-T28 | 28 | Dual-in-line <u>2/</u> |
| Y | GDIP2-F28 | 28 | Flat pack <u>2/</u> |
| Z | CGCC1-N32 | 32 | Rectangular leadless chip carrier <u>2/</u> |
| U | GDIP1-T28 or CDIP2-T28 | 28 | Dual-in-line <u>2/</u> |

1.3 Absolute maximum ratings.

| | | |
|---|-----------|------------------------|
| Supply voltage range | - - - - - | -0.5 V dc to +7.0 V dc |
| DC voltage applied to outputs in high Z state | - - - | -0.5 V dc to +7.0 V dc |
| DC input voltage | - - - - - | -3.0 V dc to +7.0 V dc |
| DC program voltage | - - - - - | 13.0 V dc |
| Maximum power dissipation (P _D) | - - - - - | 1.0 W <u>3/</u> |
| Lead temperature (soldering, 10 seconds maximum) | - - | +260°C |
| Thermal resistance, junction-to-case (θ _{JC}) | - - - - | See MIL-STD-1835 |
| Junction temperature (T _J) | - - - - - | +175°C |
| Storage temperature range | - - - - - | -65°C to +150°C |
| Temperature under bias | - - - - - | -55°C to +125°C |
| Endurance | - - - - - | 10 cycles/byte minimum |
| Data Retention | - - - - - | 10 years/minimum |

1.4 Recommended operating conditions.

| | | |
|--|-----------|----------------------|
| Supply voltage (V _{CC}) | - - - - - | 4.5 V dc to 5.5 V dc |
| Ground voltage (GND) | - - - - - | 0.0 V DC |
| Input high voltage (V _{IH}) | - - - - - | 2.0 V dc minimum |
| Input Low voltage (V _{IL}) | - - - - - | 0.8 V dc maximum |
| Case operating temperature range (T _C) | - - - - - | -55°C to +125°C |

- 1/ Generic numbers are listed on the Standardized Military Drawing Source Approval Bulletin and will also be listed in MIL-BUL-103.
- 2/ Lid shall be transparent to permit ultraviolet light erasure.
- 3/ Must withstand the added P_D due to short circuit test; (e.g., I_{OS}).

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2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
 MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.3.1 Unprogrammed devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 2. When required in groups A, B, C, or D (see 4.3), the devices shall be programmed by the manufacturer prior to test. A minimum of 50 percent of the total number of cells shall be programmed or at least 25 percent of the total number of cells to any altered item drawing.

3.2.3.2 Programmed devices. The truth tables for programmed devices shall be as specified by an attached altered item drawing.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

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TABLE I. Electrical performance characteristics.

| Test | Symbol | Conditions -55°C ≤ T _c ≤ +125°C 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified | Group A subgroups | Device type | Limit | | Unit | |
|--|------------------|---|----------------------|----------------|-------|-----|------|----|
| | | | | | Min | Max | | |
| Output high voltage | V _{OH} | V _{CC} = 4.5 V, I _{OH} = -2.0 mA, V _{IN} = V _{IH} , V _{IL} | 1,2,3 | ALL | 2.4 | | V | |
| Output low voltage | V _{OL} | V _{CC} = 4.5 V, I _{OL} = 6.0 mA, V _{IN} = V _{IH} , V _{IL} | | | | 0.4 | | |
| Input high voltage <u>1/</u> | V _{IH} | | | | 2.0 | | | |
| Input low voltage <u>1/</u> | V _{IL} | | | | | 0.8 | | |
| Input leakage current | I _{LI} | GND ≤ V _{IN} ≤ V _{CC} | | | | -10 | +10 | μA |
| Output leakage current | I _{OZ} | GND ≤ V _{OUT} ≤ V _{CC} V _{CC} = 5.5 V | | | | -40 | +40 | |
| Output short circuit current <u>2/ 3/</u> | I _{OS} | V _{CC} = 5.5 V, V _{OUT} = 0.0 V | | | | -20 | -90 | mA |
| Power supply current | I _{CC} | V _{CC} = 5.5 V, I _{OUT} = 0 mA, V _{IN} = 0 to 3.0 V, f = f _{MAX} <u>4/ 5/</u> | | | | | 130 | |
| Standby supply current | I _{SB} | V _{CC} = 5.5 V, $\overline{CS}_1 \geq V_{IH}$, I _{OUT} = 0 mA, V _{IN} = 2.0 V | | | | | 40 | |
| Input capacitance <u>3/</u> | C _{IN} | V _{CC} = 5.0 V, T = 25°C, f = 1 MHz, (see 4.3.1c) | | | 4 | | 10 | pF |
| Output capacitance <u>3/</u> | C _{OUT} | V _{CC} = 5.0 V, T = 25°C, f = 1 MHz (see 4.3.1c) | 4 | | 10 | | | |
| Functional testing | | See 4.3.1e | 7,8 | | | | | |
| Address to output valid | t _{AA} | See figures 3 and 4 and note <u>6/</u> | 9,10,11 | 01,04 | | 55 | ns | |
| | | | | 02,05 | | 45 | | |
| | | | | 03,06 | | 35 | | |

See footnotes at end of table

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|---|-------------------|-----------------------------|--------------------|
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TABLE I. Electrical performance characteristics - Continued.

| Test | Symbol | Conditions -55°C ≤ T _C ≤ +125°C 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified | Group A subgroups | Device type | Limit | | Unit |
|--|-------------------|--|----------------------|----------------|-------|-----|------|
| | | | | | Min | Max | |
| Chip select inactive to high Z (CS ₁ and CS ₂ only) <u>3/ 7/</u> | t _{HZCS} | See figures 3 and 4 and note <u>6/</u> | 9,10,11 | 01,02 | | 30 | ns |
| | | | | 03 | | 25 | |
| Output enable inactive to high Z <u>3/ 7/</u> | t _{HZOE} | | | 04 | | 30 | |
| | | | | 05,06 | | 25 | |
| Chip select active to output valid (CS ₁ and CS ₂ only) | t _{ACS} | | | 01,02 | | 30 | |
| | | | | 03 | | 25 | |
| Output enable active to output valid | t _{OE} | | | 04 | | 30 | |
| | | | | 05,06 | | 25 | |
| Chip enable inactive to high Z (CE only) <u>3/ 7/</u> | t _{HZCE} | | | 01,04 | | 60 | |
| | | | | 02,05 | | 50 | |
| | | | | 03,06 | | 40 | |
| Chip enable active to output valid (CE only) | t _{ACE} | | | 01,04 | | 60 | |
| | | | | 02,05 | | 50 | |
| | | | | 03,06 | | 40 | |
| Chip enable active to power up <u>3/</u> | t _{PU} | | ALL | | 0 | | |
| Chip enable inactive to power down <u>3/</u> | t _{PD} | 01,04 | | 60 | | | |
| | | 02,05 | | 50 | | | |
| | | 03,06 | | 40 | | | |
| Output hold from address change <u>3/</u> | t _{OH} | | ALL | | 0 | | |

- 1/ These are absolute values with respect to device ground and all overshoots and undershoots due to system or tester noise are included.
- 2/ For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed thirty seconds.
- 3/ Tested initially and after any design or process changes that affect that parameter, and therefore shall be guaranteed to the limits specified in table I.
- 4/ At f = f_{MAX}, the inputs are switching at 1/t.
- 5/ Devices 01-03 CE = 0.0 V, CS₁ = 3.0 V, CS₂ = 0.0 V; devices 04-06 CE = 0.0 V, OE = 3.0 V.
- 6/ AC tests are performed with input rise and fall times of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and the output load on figure 4, circuit A.
- 7/ Transition is measured at steady-state high level -500 mV or steady-state low level +500 mV on the output from the 1.5 V level on the input with the output load on figure 4, circuit B.

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| Device Types | 01 - 03 | | 04 - 06 | |
|-----------------|-----------------|-----------------|-----------------|-----------------|
| Case Outlines | X,Y | Z | U | Z |
| Terminal Number | Terminal Symbol | | Terminal Symbol | |
| 1 | A ₉ | NC | V _{PP} | NC |
| 2 | A ₈ | A ₉ | A ₁₂ | V _{PP} |
| 3 | A ₇ | A ₈ | A ₇ | A ₁₂ |
| 4 | A ₆ | A ₇ | A ₆ | A ₇ |
| 5 | A ₅ | A ₆ | A ₅ | A ₆ |
| 6 | A ₄ | A ₅ | A ₄ | A ₅ |
| 7 | A ₃ | A ₄ | A ₃ | A ₄ |
| 8 | A ₂ | A ₃ | A ₂ | A ₃ |
| 9 | A ₁ | A ₂ | A ₁ | A ₂ |
| 10 | A ₀ | A ₁ | A ₀ | A ₁ |
| 11 | O ₀ | A ₀ | O ₀ | A ₀ |
| 12 | O ₁ | NC | O ₁ | NC |
| 13 | O ₂ | O ₀ | O ₂ | O ₀ |
| 14 | GRND | O ₁ | GRND | O ₁ |
| 15 | O ₃ | O ₂ | O ₃ | O ₂ |
| 16 | O ₄ | GRND | O ₄ | GRND |
| 17 | O ₅ | NC | O ₅ | NC |
| 18 | O ₆ | O ₃ | O ₆ | O ₃ |
| 19 | O ₇ | O ₄ | O ₇ | O ₄ |
| 20 | CE | O ₅ | CE | O ₅ |
| 21 | CS ₂ | O ₆ | A ₁₀ | O ₆ |
| 22 | CS ₁ | O ₇ | OE | O ₇ |
| 23 | A ₁₄ | CE | A ₁₁ | CE |
| 24 | A ₁₃ | CS ₂ | A ₉ | A ₁₀ |
| 25 | A ₁₂ | CS ₁ | A ₈ | OE |
| 26 | A ₁₁ | NC | A ₁₃ | NC |
| 27 | A ₁₀ | A ₁₄ | A ₁₄ | A ₁₁ |
| 28 | V _{CC} | A ₁₃ | V _{CC} | A ₉ |
| 29 | --- | A ₁₂ | --- | A ₈ |
| 30 | --- | A ₁₁ | --- | A ₁₃ |
| 31 | --- | A ₁₀ | --- | A ₁₄ |
| 32 | --- | V _{CC} | --- | V _{CC} |

FIGURE 1. Terminal connections.

| | | | |
|---|-------------------|-----------------------------|--------------------|
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Devices 01 - 03

| State | Mode | CS ₂ | $\overline{\text{CS}}_1$ | $\overline{\text{CE}}$ | A ₁₄ - A ₀ | Power | Outputs |
|--------------|-------------------|------------------|--------------------------|------------------------|----------------------------------|-----------------|----------|
| Programmed | Read | V _{IH} | V _{IL} | V _{IL} | X | I _{CC} | Data out |
| | Standby | X | X | V _{IH} | X | I _{SB} | High Z |
| | Output disable | X | V _{IH} | X | X | I _{CC} | High Z |
| | Output disable | V _{IL} | X | X | X | I _{CC} | High Z |
| Unprogrammed | Blank check ones | V _{IHP} | V _{PP} | V _{ILP} | X | I _{CC} | Ones |
| | Blank check zeros | V _{ILP} | V _{PP} | V _{ILP} | X | I _{CC} | Zeros |

Devices 04 - 06

| State | Mode | $\overline{\text{CE}}$ | $\overline{\text{OE}}$ | V _{PP} | A ₁₄ - A ₀ | Power | Outputs |
|--------------|-------------------|------------------------|------------------------|-----------------|----------------------------------|-----------------|----------|
| Programmed | Read | V _{IL} | V _{IL} | X | X | I _{CC} | Data out |
| | Standby | V _{IH} | X | X | X | I _{SB} | High Z |
| | Output disable | X | V _{IH} | X | X | I _{CC} | High Z |
| Unprogrammed | Blank check ones | V _{IHP} | V _{ILP} | V _{PP} | X | I _{CC} | Ones |
| | Blank check zeros | V _{ILP} | V _{ILP} | V _{PP} | X | I _{CC} | Zeros |

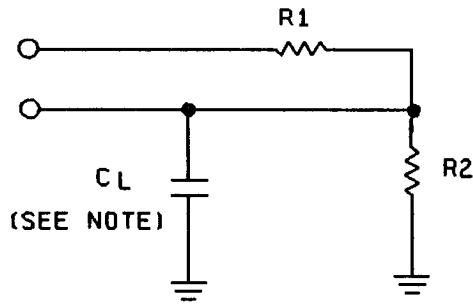
NOTES:

1. X = Don't care
2. High Z = High-impedance state

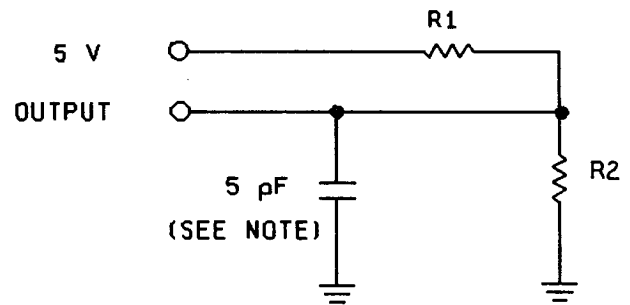
FIGURE 2. Truth table

| | | |
|---|---------------------|------------|
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Circuit A
Output load



Circuit B
Output Load for t_{HZCS} , t_{HZOE} , and t_{HZCE}

NOTE: Including scope and jig (minimum values).

| Load | Circuit A | Circuit B |
|-------|-----------|-----------|
| R1 | 658 | 658 |
| R2 | 403 | 403 |
| C_L | 30 | 5 |

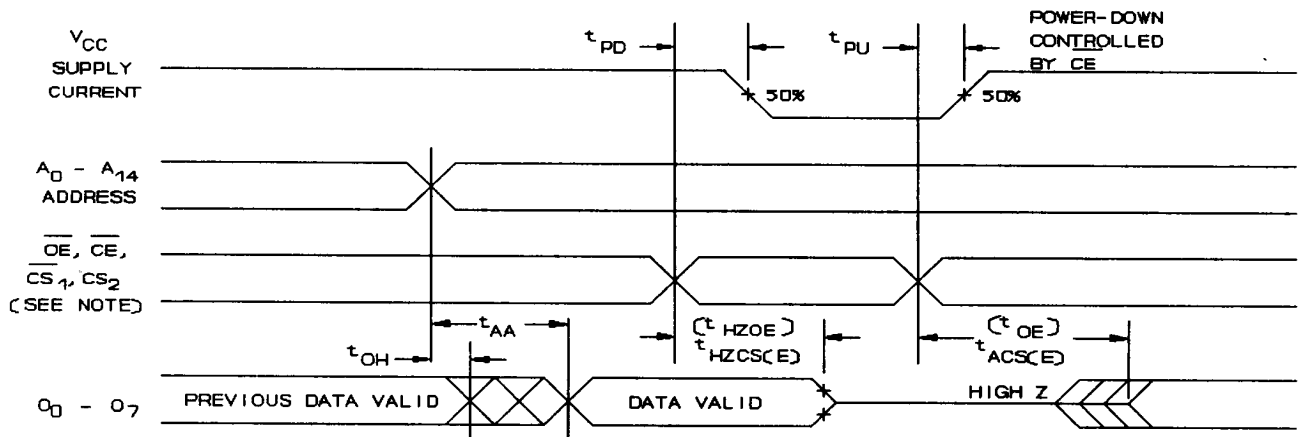
AC test conditions

| | |
|-------------------------------|--------------|
| Input pulse levels | GND to 3.0 V |
| Input rise and fall times | ≤ 5 ns |
| Input timing reference levels | 1.5 V |
| Output reference levels | 1.5 V |

FIGURE 3. Output load circuits and test conditions.

| | | | |
|---|-------------------|-----------------------------|--------------------|
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- NOTES:
1. \overline{CS}_1 and CS_2 are valid for device types 01-03 only. \overline{OE} is valid for device types 04-06 only.
 2. t_{HZOE} and t_{OE} are valid for device types 04-06 only.

FIGURE 4. Switching waveforms.

| | | | |
|---|------------------|----------------------------|-------------------|
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3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Processing EPROMs. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.10.1 Erasure of EPROMs. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.4.

3.10.2 Programmability of EPROMs. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.5.

3.10.3 Verification of erasure of programmability of EPROMs. When specified, devices shall be verified as either programmed to the specified pattern or erased. As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all cells are in the proper state. Any cell that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

- a. Burn-in test, method 1015 of MIL-STD-883.
 - (1) Test condition D using the circuit submitted with the certificate of compliance (see 3.6 herein).
 - (2) $T_A = +125^{\circ}\text{C}$, minimum.
- b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.
- c. The percent defective allowable (PDA) shall be as specified in MIL-M-38510.
- d. A data retention stress test shall be included as part of the screening procedure and shall consist of the following steps: (Steps 1 through 4 may be performed at the wafer level. The maximum storage temperature shall not exceed 200°C for packaged devices or 300°C for unassembled devices.)

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Margin test method.

- (1) Program a minimum of 50 percent of the total number of bits (see 3.10.2).
- (2) Bake, unbiased, for 72 hours at +140°C or for 48 hours at +150°C or for 8 hours at +200°C or for 2 hours at +300°C for unassembled devices only.
- (3) Test at +25°C (minimum) (see 3.10.3), including a margin test using verify mode at $V_M = +4.5$ V and loose timing (i.e., $t_{AA} = 1 \mu s$).
- (4) Erase (see 3.10.1).
- (5) Program at +25°C with a 50 percent pattern (checkerboard or equivalent).
- (6) Perform dynamic burn-in (see 4.2a).
- (7) Perform electrical tests at $T_C = +25^\circ C$, including a margin test using read mode at $V_M = +5.7$ V and loose timing (i.e., $t_{AA} = 1 \mu s$).
- (8) Perform electrical tests at $T_C = -55^\circ C$, including a margin test using read mode at $V_M = +5.7$ V and loose timing (i.e., $t_{AA} = 1 \mu s$).
- (9) Perform electrical tests at $T_C = +125^\circ C$, including a margin test using read mode at $V_M = +5.7$ V and loose timing (i.e., $t_{AA} = 1 \mu s$).
- (10) Erase (see 3.10.1). Devices may be submitted for groups A, B, C, and D testing prior to erasure provided the devices have been 100 percent seal tested in accordance with method 5004 of MIL-STD-883.
- (11) Verify erasure (see 3.10.3).

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

TABLE II. Electrical test requirements. 1/ 2/ 3/

| MIL-STD-883 test requirements | Subgroups (per method 5005, table I) |
|---|--|
| Interim electrical parameters (method 5004) | 1 |
| Final electrical test parameters (method 5004) for unprogrammed devices | 1*,2,3,7*,8 |
| Final electrical test parameters (method 5004) for programmed devices | 1*,2,3,7*,8,9 |
| Group A test requirements (method 5005) | 1,2,3,4**,7, 8,9,10,11 |
| Groups C and D end-point electrical parameters (method 5005) | 2,3,7,8A,8B |

1/ * Indicates PDA applies to subgroups 1 and 7.

2/ Any or all subgroups may be combined when using high-speed testers.

3/ ** see 4.3.1c.

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| STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444 | SIZE A | | 5962-89817 |
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4.3.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.
- c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured for the initial characterization and after any process or design changes which may affect capacitance. Sample size is 15 devices with no failures, and all input and output terminals tested.
- d. All devices selected for testing shall be programmed with a checkerboard pattern or equivalent.
- e. Subgroups 7 and 8 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test conditions, method 1005 of MIL-STD-883.
 - (1) Test condition D using the circuit submitted with the certificate of compliance (see 3.6 herein).
 - (2) $T_A = +125^\circ\text{C}$, minimum.
 - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4 Erasing procedure. The recommended erasure procedure for the device is exposure to shortwave ultraviolet light which has a wavelength of 2537 angstroms (\AA). The integrated dose time (i.e., UV intensity x exposure time) for erasure should be a minimum of 25 Ws/cm^2 . The erasure time with this dosage is approximately 35 minutes using a ultraviolet lamp with a $12,000 \mu\text{W/cm}^2$ power rating. The device should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose the device can be exposed to without damage is 7258 Ws/cm^2 (1 week at $12,000 \mu\text{W/cm}^2$). Exposure of devices to high intensity UV light for long periods may cause permanent damage.

4.5 Programming procedures. The programming procedures shall be as specified by the device manufacturer.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECS, telephone (513) 296-6021.

6.5 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5377.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECS.

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